7. The device of claim 1, wherein the device isolation region comprises a deep trench isolation region.

8. The device of claim 1, wherein the device isolation region comprises:

a pair of deep trench isolation regions; and

a conductive region disposed between the pair of deep trench isolation regions and electrically connected to the semiconductor substrate and a ground terminal.

9. The device of claim 1, wherein the drift region does not extend laterally across an entire lateral extent of the drain region.

10. The device of claim 1, wherein:

the drift region comprises an outer section and an inner section surrounded by the outer section and disposed under the drain region; and

the inner section is diminished relative to the outer section such that full depletion of the drift region is attainable during operation.

11. An electronic apparatus comprising:

a semiconductor substrate; and

a transistor disposed in the semiconductor substrate and comprising:

first and second semiconductor regions having a first conductivity type;

a third semiconductor region having a second conductivity type and through which current flows between the first and second semiconductor regions during operation;

a device isolation region laterally surrounding the first, second, and third semiconductor regions;

a breakdown protection region disposed between the device isolation region and the third semiconductor region and having the first conductivity type; and

a buried layer extending laterally across the first semiconductor region, the second semiconductor region, and the third semiconductor region and having the second conductivity type;

wherein the breakdown protection region has a width at a surface of the semiconductor substrate in a lateral direction that establishes a spacing between the third semiconductor region and the device isolation region, the width falling in a range from 1.0 microns to 2.0 microns so that the breakdown protection region improves a breakdown voltage level of the transistor by preventing charge inversion from occurring in the third semiconductor region along the device isolation region;

wherein the breakdown protection region is electrically floating; and

wherein the first conductivity type is p-type and the second conductivity type is n-type.

12. The electronic apparatus of claim 11, wherein the breakdown protection region is disposed along, and contiguous with, an inner boundary of the device isolation region.

13. The electronic apparatus of claim 11, further comprising a buried oxide layer disposed in the semiconductor substrate, over which the buried layer is disposed, and disposed at a depth to which the device isolation region reaches, wherein the semiconductor substrate comprises an epitaxial layer over the buried oxide layer in which the first semiconductor region, the second semiconductor region, the third semiconductor region, and the breakdown protection region are disposed.

14. The electronic apparatus of claim 11, wherein the transistor is configured as a reduced surface field (RESURF) transistor.

15. The electronic apparatus of claim 11, wherein the breakdown protection region comprises a ring-shaped well disposed between the device isolation region and the third semiconductor region.

16. The electronic apparatus of claim 11, wherein the transistor further comprises a doped buried layer that extends laterally across the transistor to provide isolation along a lower boundary of the transistor, wherein the breakdown protection region has a lower boundary contiguous with the doped buried layer.

17. The device of claim 1, wherein the well is ring-shaped.

18. The device of claim 1, further comprising a doped buried layer that extends laterally across a device area to provide isolation along a lower boundary of the device, wherein the well has a lower boundary contiguous with the doped buried layer.

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